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integrated circuit, there being a conductive via or stud in said flowable oxide insulator layer that electrically connects said two non coplanar metal layers.

48. (New) The integrated circuit of claim 47, wherein said via or stud is surrounded by said thin oxidized surface layer.

REMARKS

Applicant cancelled claims 34-35, amended claims 32-33 to recite "primary protective layer", and added new claims 36-48. Thus, Applicant believes the claims objections and rejections under § 112 are overcome.

Rejections Under 35 USC §102 / §103

Applicant respectfully traverses the Examiner's rejection of claims 27-33.

In Bia et al, flowable oxide is not specifically cited. Mostly ceramic examples are given in Bia et al, so there is no recognition of the problem when a "flowable oxide" is used. Applicant claims a "flowable oxide" (e.g., claim 27).

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In Bia et al, the primary barrier is the blocking layer 42, which is SiNx or a conductive material such as Ta, TaN, ... Col. 5, lines 29+.

Applicant claims a thin oxided layer of the flowable oxide as the primary barrier. This thin layer can be formed by a plasma treatment of the flowable oxide and is sufficiently thin that the dielectric constant remains very low. The unexpected result is that a thin oxidized layer provides the barrier properties while not adversely affecting the dielectric constant.

In Lopatin et al, a flowable oxide is not mentioned, hence the problem concerning a "flowable oxide" is not recognized.

The "first barrier" is the seed layer 124, which obviously is not a barrier to the conductor. The "second barrier" is the conductive layer 123. Both "barriers" are continuous along the sides and bottom of a trench in which the conductor is located. Thus, Lopatin et al does not recognize the problem and does not provide a thin oxide barrier.

No reference cited (e.g., Bia et al, Lopatin et al, Yew et al, Kawanoue et al, or Ashley et al) teaches, discloses or suggests that a thin oxide of the flowable oxide insulator is a good barrier.

Entry of this amendment, allowance of claims 27-33, 36-48 are solicited.

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Attached hereto is a marked-up version of the changes made to the claims by the current amendment. **This appendix is captioned "Version with Markings to Show Changes Made".**

For the foregoing reasons, allowance of the claims is respectfully solicited.

Respectfully submitted,
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Attachment: Appendix - Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 27, 28, 29, 31, 32, 33 have been amended as follows:

27. (Amended) An integrated circuit semiconductor device including

a substrate having a substrate surface,

a flowable oxide insulator (FOX) layer upon said substrate surface,

a trough in said flowable oxide insulator layer,

sidewalls of said flowable oxide insulator layer,

a primary protective layer on said sidewalls of said flowable oxide insulator layer, said primary protective layer being a thin oxidized surface of said FOX, said thin surface layer preventing the exposure of said flowable oxide insulator layer to moisture and lithographic resist developers, said primary protective layer being substantially impervious to copper extrusion, and

a secondary protective layer on said primary protective layer and on said substrate surface, said secondary protective layer being electrically conductive.

28. (Amended) The integrated circuit semiconductor device as claimed in claim 27, further comprising,

[an oxidized FOX layer upon said flowable oxide insulator layer,]

an oxide layer upon said oxidized FOX layer,

a conductor in said trough, said conductor and said oxide layer forming a[an even] planar surface, said conductor being in electrical communication with said secondary protective layer,

and

a nitride layer upon said [even]planar surface.

29. (Amended) The integrated circuit semiconductor device a claimed in claim 28, further comprising a [second]damascene layer, said [second]damascene layer comprising,

another flowable oxide insulator (FOX) layer upon said nitride layer,

another thin oxidized surface layer of said another [oxidized]FOX layer [upon said another flowable oxide insulator layer],

another trough in said another FOX layer,

another sidewalls of said another flowable oxide insulator layer in said another trough,

another primary protective layer upon said another sidewalls, said another primary protective layer being said another thick oxidized surface layer preventing the exposure of said another flowable oxide insulator layer to moisture and lithographic resist developers, said another primary protective layer being impervious to copper extrusion,

another secondary protective layer upon said another primary protective layer and upon said even planar surface, said another secondary protective layer being in electrical communication with said conductor, and

another conductor in said another trough, said another conductor being in electrical communication with said another secondary protective layer.

31. (Amended) The integrated circuit semiconductor device as claimed in claim 27, further comprising a nitride supplemental protective layer on said primary protective layer [said supplemental protective layer being impervious to moisture, lithographic resist developers, and copper extrusion, said supplemental protective layer improving adhesion with a metallic conductor]for improving adhesion with a metallic conductor.

32. (Amended) The integrated circuit semiconductor device as claimed in claim 27, wherein said [first]primary layer is a barrier layer.

33. (Amended) The integrated circuit semiconductor device as claimed in claim 27, wherein said [first]primary protective layer on said sidewalls of said flowable oxide insulator layer has a thickness equal to or less than 20% of a thickness of said flowable oxide insulator layer

Claims 34 and 35 have been canceled.

New claims 36-48 have been added.

36. (New) The integrated circuit device of claim 31, wherein said supplemental protective layer is a nitride layer.

37. (New) The integrated layer of claim 27, wherein said thin layer of plasma-formed oxide has a thickness not exceeding about 500 Å.

38. (New) An integrated circuit including

a layer of flowable oxide insulator, and

a thin protective layer thereon, said thin protective layer being an oxidized surface layer of said flowable oxide insulator that is resistant to moisture and lithographic resist developers.

39. (New) The integrated circuit of claim 38, wherein said thin oxidized layer has a thickness less than about 500 Å.

40. (New) The integrated circuit of claim 38, wherein said thin oxidized layer is a plasma-formed layer.

41. (New) The integrated circuit of claim 38, further including a nitride or oxynitride layer on said thin oxidized surface layer.

42. (New) The integrated circuit of claim 38, further including a deposited oxide layer deposited on said thin oxidized surface layer.

43. (New) The integrated circuit of claim 38, further including a conductive layer on said thin oxidized surface layer.

44. (New) The integrated circuit of claim 43, further including a metal conductor in contact with said conductive barrier layer.

45. (New) The integrated circuit of claim 44, wherein said metal conductor contains copper.

46. (New) The integrated circuit of claim 45, wherein said conductive barrier layer includes a refractory metal or alloy.

47. (New) The integrated circuit of claim 46, wherein said layer of flowable oxide insulator is located between two non coplanar metal layers used for interconnections in said integrated circuit, there being a conductive via or stud in said flowable oxide insulator layer that electrically connects said two non coplanar metal layers.

48. (New) The integrated circuit of claim 47, wherein said via or stud is surrounded by said thin oxidized surface layer.